REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1 and 3-26 remain in the application. Claims 1, 3-5, and 21-22 have been amended. Claim 2 has been cancelled.

In item 2 on page 2 of the above-mentioned Office action, claims 1-16 and 19-20 have been rejected as being anticipated by An (US 5,624,862) under 35 U.S.C. § 102(b).

In item 23 on page 9 of the above-mentioned Office action, claims 17-18 have been rejected as being unpatentable over An in view of Azmanov (US 5,517,061) under 35 U.S.C. § 103(a).

In item 26 on page 10 of the above-mentioned Office action, claims 21-26 have been rejected as being unpatentable over An in view of Camerlenghi et al. (US 6,124,169) under 35 U.S.C. § 103(a).

The rejections have been noted and claims 1, 5, and 21-22 have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes to claims 1 and 21 is found in original claim 2 and support

for the changes to claims 5 and 22 is found on page 42, line 23 to page 43, line 12 of the specification.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claims 1 and 21 call for, inter alia:

> removing the isolating layer completely from the bitlines at portions not covered by the wordlines with areas between the bitlines remaining unaffected, carrying out the step of removing the isolating layer from the bitlines by:
>
> depositing a photoresist material;
>
> patterning the photoresist material using a mask ~~having a stripe pattern; and~~
>
> selectively etching the isolating layer with respect to the wordlines.

Claims 5 and 22 call for, inter alia:

> removing the first isolating layer from the bitlines by a step in which also a topmost of the at least one second isolating layer is removed from the memory cell array at portions not covered by the wordlines, carrying out the removing step by:
>
> depositing a phtoresist material;
>
> photolithographically patterning the photoresist material causing the photoresist material to be removed within the memory cell array but remain in a peripheral portion of the array; and
>
> selectively etching each of the second and first isolation layers causing the isolation layer to be completely removed from the bitlines in areas not covered by the word lines.

The invention of the instant application relates to a method for providing bit line contacts in a memory cell array. A plurality of bit lines is disposed in a first direction while a plurality of word lines is disposed in a second direction. The word lines cross the bit lines at a position above the bit lines. The bit lines are isolated from the word lines by an isolation layer, which covers the bit lines.

One concept of the invention of the instant application is that the isolation layer, which may be a bit line oxide covering the bit line, is removed from the bit line in a self-adjusted manner, namely an etch step of this isolation layer is performed, which includes selectivity with respect to the word lines. For example, the word lines may have a cap nitride. In this case the bit line oxide is etched with selectivity against this cap nitride. Consequently, the isolation layer is completely removed from the bit lines in areas, which are not covered by word lines.

The two aspects provided in claims 1 and 5, respectively, or 21 and 22 with regard to the NROM chip, achieve this by either providing a mask having stripes along the bit lines or having a fully transparent field with respect to the memory cell area. In both cases, the isolation layer is removed from the bit lines exactly in those areas not covered by the word

lines. A difference resides in the treatment of that area, which is neither covered by the word line nor by the bit line:

- according to the first aspect, the isolation layer in this area is masked by the striped mask (which may be the same mask as the bit line generating mask);
- according to the second aspect, the isolation layer (herein the ONO layer) is also removed from this area.

It is further noted that instead of using a resist (17) according to the first aspect, the second aspect deals with a second isolation layer (16, 22) in order to protect gate electrodes, ~~which are arranged in a periphery of the chip,~~ against oxide or nitride etches applied to the memory array. This second layer is also deposited within the memory cell array and particularly on the substrate between the bit lines, where it is to be removed according to the second aspect of the invention of the instant application.

An describes a method of making a mask ROM. A plurality of bit lines (considered as active region 210 between field oxides films 110 in Fig. 2) and word lines (gate electrodes 13) are formed. The bit lines 18 (see Fig. 4F) according to An are comparable with the metal lines of the invention of the instant application. Bit lines 210 and word lines 13 cross each other (see Fig. 2 of An). Memory cells 111, 112, 113 are

disposed at respective cross points. An isolation layer (insulation film 17) covers the bit lines (active regions 210; Fig. 2 and Fig. 4F). A contact hole 19 is formed within this isolation layer 17, which is then filled with a conductive bit line material (numeral 18, which is metal here, and not a diffusion strip, see discussion above).

In contrast to the invention of the instant application, the insulation film 17 according to An is not removed completely from the bit lines (active region 210) in areas, which are not covered by the word lines 13. Fig. 4F shows that the bit line area is larger than the resulting contact hole 19 area. Further, there is no mention in An of a selective etch with respect to the word lines. The corresponding paragraph (column 4, lines 10 - 15) suggests that a conventional contact hole pattern mask is employed to open the isolation layer. The use of a stripe pattern photo mask or a photo mask, which fully exposes the memory cell area while the periphery is masked with a resist, is neither explicitly nor implicitly indicated in An.

Azmanov discloses a CMOS based ROM. The teachings of a self-aligned removal of an insulation layer specifically from a bit line not covered by a word line, cannot be found in Azmanov (particularly not in the corresponding paragraph at column 10,

lines 8-21). The same is true for Camerlenghi et al. who disclose the formation process of a contact structure in nonvolatile memory devices.

The particular advantages of the invention of the instant application are pointed out on page 10, line 21 to page 11, line 12 of the specification of the instant application, where it is stated with regard to the first aspect that, e.g., the stripe pattern used for the mask offers reusing the bit line mask for opening the isolation layer - a fact, which makes alignment of mask patterns much easier. Misalignment is then avoided. With regard to the second aspect, a mask only defining the extent of the whole memory cell array (versus the peripheral chip area) and not the contact hole structures is necessary (see page 12, lines 6-13 of the specification). As a result, removal of the bit line oxide is no longer a critical step.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1, 5, and 21-22. Claim 1, 5, and 21-22 are, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claims 1, 5, 21, or 22, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1 and 3-26 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicants

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June 30, 2005

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